NECST Talk during NGC2017

.:: Thursday 1 June, 2017 ::.
NGC17 - NECST Lab visiting Bloomberg
- A Scalable Dataflow Implementation of Curran's Approximation Algorithm, by Anna Maria Nestorov, MSc student in CE at Politecnico di Milano
- Self-adaptive container monitoring with performance-aware Load-Shedding policies, by Rolando Brondolin, PhD student in System Architecture at Politecnico di Milano

.:: Monday 5 June, 2017 ::.
NGC17 - NECST Lab visiting Lawrence Berkeley National Laboratory
- XeMPUPiL: Towards Performance-aware Power Capping Orchestrator for the Xen Hypervisor, by Marco Arnaboldi MSc student in CE at Politecnico di Milano
- Long Read Overlap Discovery through Sparse Matrix Multiplication, by Giulia Guidi, MSc student in BioMed engineering at Politecnico di Milano and visiting student at Lawrence Berkeley National Laboratory
- Data Analytics for HPC, by Costin Iancu, Lawrence Berkeley National Laboratory
- Exploit FPGA-based Systems from Data Science High Level Languages, by Luca Stornaiuolo, MSc student in CE at Politecnico di Milano
- CNN Dataflow Implementation on FPGAs, by Marco Bacis, MSc student in CE at Politecnico di Milano
Fast Algorithms for Quantized Convolutional Neural Networks, by Alessandro Pappalardo, MSc student in CE at Politecnico di Milano
- HUGenomics: a support for personalized medicine research, by Lorenzo Di Tucci, PhD student in System Architecture at Politecnico di Milano
- Architectural Optimizations for High Performance and Energy Efficient Smith-Waterman Implementation on FPGAs Using OpenCL, by Lorenzo Di Tucci, PhD student in System Architecture at Politecnico di Milano
- Hardware Acceleration of Genetic Variant Caller: A Support for Personalized Medicine, by Chiara Crippa, MSc student in BioMed engineering at Politecnico di Milano
- TiReX: a Tiled Regular eXpression matching architecture, by Alessandro Comodi and Davide Conficconi, MSc students in CE at Politecnico di Milano
- A Highly Parallel Semi-Dataflow FPGA Architecture for Large-Scale N-Body Simulation, by Emanuele Del Sozzo, PhD student in System Architecture at Politecnico di Milano

NGC17 - NECST Lab visiting Pinterest
- Learning by s/doing/h4ck1ng/ - Our experience learning application security through hacking competitions, Marcello Pogliani, PhD student in System Security at Politecnico di Milano
- Self-adaptive container monitoring with performance-aware Load-Shedding policies, by Rolando Brondolin, PhD student in System Architecture at Politecnico di Milano

.:: Tuesday 6 June, 2017 ::.
NGC17 - NECST Lab visiting Sysdig
- Self-adaptive container monitoring with performance-aware Load-Shedding policies, by Rolando Brondolin, PhD student in System Architecture at Politecnico di Milano
- System Security @ NECSTLab and Breaking the Laws of Robotics: Attacking Industrial Robots

NGC17 - NECST Lab visiting Quid
- CNNECST: an FPGA-based approach for the hardware acceleration of Convolutional Neural Networks, by Emanuele Del Sozzo, PhD student in System Architecture at Politecnico di Milano
- CNN Dataflow Implementation on FPGAs, by Marco Bacis, MSc student in CE at Politecnico di Milano
- Exploit FPGA-based Systems from Data Science High Level Languages, by Luca Stornaiuolo, MSc student in CE at Politecnico di Milano

.:: Wednesday 7 June, 2017::.
NGC17 - NECST Lab visiting Microsoft
- NECSTLab and Microsoft, by Marco Santambrogio, Assistant Professor at Politecnico di Milano
- ShieldFS: The Last Word in Ransomware Resilient Filesystems, by Andrea Continella, PhD student in System Security at Politecnico di Milano
- Self-adaptive container monitoring with performance-aware Load-Shedding policies, by Rolando Brondolin, PhD student in System Architecture at Politecnico di Milano
- Exploit FPGA-based Systems from Data Science High Level Languages, by Luca Stornaiuolo, MSc student in CE at Politecnico di Milano
- Fast Algorithms for Quantized Convolutional Neural Networks, by Alessandro Pappalardo, MSc student in CE at Politecnico di Milano

NGC17 - NECST Lab visiting Oracle
- Self-adaptive container monitoring with performance-aware Load-Shedding policies, by Rolando Brondolin, PhD student in System Architecture at Politecnico di Milano
- XeMPUPiL: Towards Performance-aware Power Capping Orchestrator for the Xen Hypervisor, by Marco Arnaboldi MSc student in CE at Politecnico di Milano
- CNNECST: an FPGA-based approach for the hardware acceleration of Convolutional Neural Networks, by Emanuele Del Sozzo, PhD student in System Architecture at Politecnico di Milano
- CNN Dataflow Implementation on FPGAs, by Marco Bacis, MSc student in CE at Politecnico di Milano
- Fast Algorithms for Quantized Convolutional Neural Networks, by Alessandro Pappalardo, MSc student in CE at Politecnico di Milano
- Architectural Optimizations for High Performance and Energy Efficient Smith-Waterman Implementation on FPGAs Using OpenCL (10’), by Lorenzo Di Tucci, PhD student in System Architecture at Politecnico di Milano
- Exploit FPGA-based Systems from Data Science High Level Languages, by Luca Stornaiuolo, MSc student in CE at Politecnico di Milano

- TiReX: a Tiled Regular eXpression matching architecture, by Alessandro Comodi and Davide Conficconi, MSc students in CE at Politecnico di Milano

.:: Thursday 8 June, 2017 ::.
NGC17 - NECST Lab visiting Xilinx
- NECST at a Glance and the DReAMS Research Line, by Marco Santambrogio, Assistant Professor at Politecnico di Milano
- CAOS: A CAD Framework for FPGA-Based Systems, by Marco Rabozzi, PhD student in System Architecture at Politecnico di Milano
- Deep Learning Initiative @ NECSTLab, by Emanuele Del Sozzo, PhD student in System Architecture at Politecnico di Milano
- FPGA-enhanced Bioinformatics @ NECST, by Lorenzo Di Tucci, PhD student in System Architecture at Politecnico di Milano
- Pearson Correlation Coefficient acceleration for modelling and mapping of neural interconnections, Enrico Reggiani, MSc student in EE at Politecnico di Milano
- NOMICA, Chiara Crippa, MSc student in BioMed engineering at Politecnico di Milano
- ProFAX: a hardware acceleration of a protein folding algorithm, Giulia Guidi, MSc student in BioMed engineering at Politecnico di Milano
- CNN Dataflow implementation on FPGAs, Marco Bacis, MSc student in CE at Politecnico di Milano
- Fast algorithms for quantised convolutional neural networks, Alessandro Pappalardo, MSc student in CE at Politecnico di Milano
- Exploiting FPGAs from Higher Level Languages (A signal analysis case study), Luca Stornaiuolo, MSc student in CE at Politecnico di Milano
- numPYNQ: An accelerate version of NumPy for PYNQ platform, Luca Stornaiuolo, MSc student in CE at Politecnico di Milano
- Roofline Model for FPGA: A tool for Performance Analysis and Application Optimization, Francesco Bertelli, MSc student in CE at Politecnico di Milano
- TiReX: a Tiled Regular eXpression matching architecture, Davide Conficconi + Alessandro Comodi, MSc student in CE at Politecnico di Milano
- A Scalable Dataflow Implementation of Curran's Approximation Algorithm, by Anna Maria Nestorov, MSc student in CE at Politecnico di Milano

.:: Friday 9 June, 2017 ::.
NGC17 - NECST Lab visiting Samsung Research America
- A wearable device for color perception restoration in blind people, by Luca Cerina, RA at NECST Lab, Politecnico di Milano
- Reconfigurable Embedded Systems Applications for Versatile Biomedical Measurements, by Luca Cerina, RA at NECST Lab, Politecnico di Milano
- Relationships between heart-rate variability and pulse-rate variability obtained from video-PPG signal using ZCA, by Luca Cerina, RA at NECST Lab, Politecnico di Milano
- ShieldFS: The Last Word in Ransomware Resilient Filesystems, by Andrea Continella, PhD student in System Security at Politecnico di Milano
- Obfuscation-Resilient Privacy Leak Detection for Mobile Apps, by Andrea Continella, PhD student in System Security at Politecnico di Milano

- Exploit FPGA-based Systems from Data Science High Level Languages, by Luca Stornaiuolo, MSc student in CE at Politecnico di Milano
- CNNECST: an FPGA-based approach for the hardware acceleration of Convolutional Neural Networks, by Emanuele Del Sozzo, PhD student in System Architecture at Politecnico di Milano
- CNN Dataflow Implementation on FPGAs, by Marco Bacis, MSc student in CE at Politecnico di Milano