PREMI RICEVUTI DAL LABORATORIO NECTS

- PREMI XOHW

La Xilinx ha organizzato la seconda edizione dello Xilinx Open Hardware Contest (http://www.openhw.eu/), competizione di livello europeo a cui hanno partecipato più di 100 team.

Il Laboratorio NECST ha avuto 4 team finalisti:

- Giuseppe Natale, PhD al primo anno, "exaFPGA: Iterative stencil cell loop acceleration";
- Giulia Guidi, MSc in ing. Biomedica, e Lorenzo Di Tucci, MSc in Ing. Informatica, "ProFAX: Protein folding on FPGA";
- Marco Bacis, studente terzo anno Ing. Informatica, Lara Cavinato, studentessa terzo anno Ing. Biomedica, e Irene Fidone, studentessa terzo anno Ing. Biomedica, "BEye: Zynq based retinal vessel segmentation";
- Enrico Reggiani, MSc in Ing. Elettronica, Marco Gucciardi, studente terzo anno Ing. Biomedica, e Eleonora D'Arnese, studentessa terzo anno Ing. Biomedica, "Brain NE(CS)Twork on FPGA".

Vi erano due categorie: FPGA category e Embedded Category.

Per ogni categoria erano assegnati due premi: uno per i PhD e uno per gli studenti di triennale o master.

Sui quattro premi complessivi, il laboratorio NECST ne ha vinti due:

- Premio per la categoria PhD nella FPGA category: Giuseppe Natale, PhD al primo anno, "exaFPGA: Iterative stencil cell loop acceleration";
- Premio per la categoria studenti nella FPGA category: Giulia Guidi, MSc in ing. Biomedica, e Lorenzo Di Tucci, MSc in Ing. Informatica, "ProFAX: Protein folding on FPGA".

- Premio a RAW

Il Laboratorio NECST ha vinto la best demo a RAW (23rd Reconfigurable Architectures Workshop), con la demo del paper:

E. Del Sozzo and A. Solazzo and A. Miele and M. D. Santambrogio, "On the Automation of High Level Synthesis of Convolutional Neural Networks". In 2016 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), RAW, Chicago, 2016, pp 217-224.

- Lavoro del NECST selezionato per "SIGDA University Demonstration at DAC"

ProFAX, il lavoro fatto da Marco Santambrogio insieme a Giulia Guidi (MSc in ing. Biomedica) e Lorenzo Di Tucci (MSc in Ing. Informatica) è stato selezione per essere presentato a SIGDA University Demonstration a DAC (@Austin, 7 June 2016). Il video del lavoro può essere trovato qui:

https://www.youtube.com/watch?v=KdsHNA39BNw&feature=youtu.be

- Talk

- Rolando Brondolin: “FFWD: latency-aware event stream processing via domain-specific load-shedding policies” - @ Sysdig, San Francisco, CA, USA - 31 May, 2016;
- Marco D. Santambrogio: “The NECST experience” - @ Oracle Labs, Redwood Shores, CA - 1 June, 2016;
- Giuseppe Natale: “A methodology and a framework for automatic dataflow implementation of Iterative Stencil Loops on a multi-FPGA system” - @ Oracle Labs, Redwood Shores, CA - 1 June, 2016;
- Rolando Brondolin: “FFWD: latency-aware event stream processing via domain-specific load-shedding policies” - @ Oracle Labs, Redwood Shores, CA - 1 June, 2016;
- Matteo Ferroni: "Data-driven power-awareness: a holistic approach" - @ Oracle Labs, Redwood Shores, CA - 1 June, 2016;
- Andrea Cirigliano: “BlueSentinel: Occupancy Detection and Monitoring for Smart buildings using Bluetooth Low Energy” @ Shopkick, Redwood City, CA - 1 June, 2016;
- Rolando Brondolin: “FFWD: latency-aware event stream processing via domain-specific load-shedding policies” @ Microsoft Research, Mountain View, CA, USA - 2 June, 2016;
- Simone Mosciatti: “Estimating time to completion for MapReduce jobs: the MARC approach” @ Microsoft Research, Mountain View, CA, USA - 2 June, 2016;
- Emanuele Del Sozzo: “Improving data locality of stencil-like MapReduce jobs” @ Microsoft Research, Mountain View, CA, USA - 2 June, 2016;
- Andrea Damiani, Andrea Corna: “A scalable framework for resource consumption modelling: the MARC approach” @ Microsoft Research, Mountain View, CA, USA - 2 June, 2016;
- Amedeo Asnaghi, "DockerCap - A software-level power capping orchestrator for Docker containers", @ Microsoft Research, Mountain View, CA, USA - 2 June, 2016;
- Simone Mosciatti: “Estimating time to completion for MapReduce jobs: the MARC approach” @ Microsoft Research, Mountain View, CA, USA - 2 June, 2016;
- Marco D. Santambrogio: “NECST and Xilinx: an interesting history” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Giuseppe Natale: “A methodology and a framework for automatic dataflow implementation of Iterative Stencil Loops on a multi-FPGA system” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Lorenzo Di Tucci: “ProFAX: a hardware acceleration of a protein folding algorithm” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Anna Maria Nestorov: “NECSTrade: An FPGA based financial friendly system” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Enrico Reggiani: “BrainNECST Work” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;

- Andrea Solazzo: “CNNECST” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Gianluca Durelli: “Increasing Power Efficiency in Asymmetric Multicores by adapting to application goals” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Luca Cerina: “SynCH - Synergically Controlled Hand” @ Xilinx, San Jose’, CA, USA - 2 June, 2016;
- Matteo Ferroni: "Data-driven power-awareness: a holistic approach" @ Facebook, Menlo Park, CA, USA - 3 June, 2016;
- Federico Maggi: “Grab ’n Run: Secure and Practical Dynamic Code Loading for Android Applications” @ Facebook, Menlo Park, CA, USA - 3 June, 2016;
- Giuseppe Natale: “A framework for automatic dataflow implementation of Iterative Stencil Loops on FPGA devices” @ Facebook, Menlo Park, CA, USA - 3 June, 2016;
- Andrea Solazzo: “CNNECST” @ Facebook, Menlo Park, CA, USA - 3 June, 2016;
- Mario Polino: “Jackdaw: Automated Reverse Engineering of Malicious Behaviors” @ Facebook, Menlo Park, CA, USA - 3 June, 2016;
- Gabriele Pallotta: “Increasing Power Efficiency in Asymmetric Multicores by adapting to application goals” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Emanuele Del Sozzo: “Increasing power efficiency in asymmetric multicores by adapting to application goals” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Giulia Guidi: “ProFAX: a hardware acceleration of a protein folding algorithm” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Anna Maria Nestorov: “All of us will be able to trade with NECSTrade” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Enrico Reggiani: “BrainNECST Work” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Luca Cerina: “SynCH - Synergically Controlled Hand” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Andrea Solazzo: “CNNECST” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Giuseppe Natale: “A methodology and a framework for automatic dataflow implementation of Iterative Stencil Loops on a multi-FPGA system” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Matteo Ferroni, "A journey towards power-awareness" @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Andrea Corna & Andrea Damiani & Matteo Ferroni, "Past, present and Future of Marc & Xarcc" @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;

- Amedeo Asnaghi: “DockerCap: orchestrating power capping of Docker containers, at the software-level” @ SWARM Lab, University of Berkeley, Berkeley, CA, USA - 6 June, 2016;
- Matteo Ferroni: "Data-driven power-awareness: a holistic approach" @ Google, Mountain View, CA, USA - 7 June, 2016;
- Luca Cerina: “PhysioC.A.M.: Contactless Acquisition Methods for connected healthcare” @ Google, Mountain View, CA, USA - 7 June, 2016;
- Chengyu Zheng: “OpenST - On-Chip System Call Tracing: A Feasibility Study and Open Prototype” @ Google, Mountain View, CA, USA - 7 June, 2016;
- Giuseppe Natale: “A framework for automatic dataflow implementation of Iterative Stencil Loops on FPGA devices” @ Google, Mountain View, CA, USA - 7 June, 2016;
- Matteo Ferroni: “NECST @ a Glance” @Center for the Built Environment - University of California, Berkeley, CA, USA - 7 June, 2016;
- Piercarlo Serena: “ThermoSense, an energy-efficient complaint-based approach for thermal comfort control” @Center for the Built Environment - University of California, Berkeley, CA, USA - 7 June, 2016;
- Andrea Cirigliano: “BlueSentinel: Real-Time Occupancy Monitoring for Smart Buildings based on Bluetooth Low Energy” @Center for the Built Environment - University of California, Berkeley, CA, USA - 7 June, 2016.