**Ph.D. in Information Technology**
**Thesis Defense**

**September 14th, 2026**
**At 02:30 p.m.**
**Room Alpha - Building 24**

**Leonardo NASSI** – 38th Cycle

**DEVELOPMENT OF READOUT ASIC FOR TOF-PET MEASUREMENT APPLIED IN RANGE MONITORING IN HADRONTHERAPY**
Supervisor: Prof. Carlo Ettore Fiorini

**Abstract:**

Time-of-Flight Positron Emission Tomography (TOF-PET) is emerging as a powerful technique for range monitoring in hadrontherapy, enabling improved accuracy in dose delivery by exploiting the temporal correlation of annihilation photons. Meeting the stringent requirements on timing resolution, energy resolution, and rate capability in TOF-PET systems poses significant challenges to the front-end electronics, particularly in the readout of silicon photomultipliers (SiPMs), which are characterized by fast signal dynamics, wide dynamic range, and non-ideal effects such as dark count rate, baseline fluctuations, and amplitude-dependent timing walk. In the specific context addressed in this work, the TOF-PET system is based on monolithic scintillation crystals coupled to SiPM arrays, rather than on conventional pixelated scintillator matrices. This architectural choice enables continuous three-dimensional interaction positioning through light distribution analysis, but introduces additional constraints on the front-end electronics, which must correctly process charge signals that are intrinsically shared among multiple channels. This doctoral dissertation presents the design, implementation, and characterization of MAGIC, a multi-channel readout ASIC specifically developed for TOF-PET applications in the context of range monitoring in hadrontherapy. The ASIC is implemented in a 110 nm CMOS technology and integrates ten fully synchronized channels optimized for the readout of monolithic scintillation crystals coupled to SiPM arrays. Each channel features a low-noise current mode input stage, a gated integrator based energy rocessing chain, dedicated baseline holders, and a high-speed timing path. A key contribution of this work is the adoption of a gated integrator architecture for energy measurement, which effectively mitigates ballistic deficit and pile-up effects while allowing flexible and programmable control of the integration window through on-chip digital logic. The timing path is based on fast comparators and a robust event validation chain comprising programmable delay elements, a DCVSL-based differential AND gate, and an LVDS output stage, ensuring reliable operation in a noisy mixed-signal environment. To address the intrinsic amplitude walk associated with leading-edge discrimination, an alternative timing technique is proposed and implemented. This approach is particularly motivated by the use of monolithic scintillators, where the scintillation light generated by a single gamma interaction is distributed across multiple SiPM channels. In this mode, the signals from all channels are attenuated, summed through a dedicated on-chip sum channel, and processed by a single comparator, enabling the reconstruction of the total collected charge. This global signal is essential

to properly capture the full light yield of the monolithic crystal and to reduce the dependence of the extracted timing information on the spatial distribution of the light and on the signal amplitude of individual channels. In this mode, signals from all channels are attenuated, summed, and processed by a single comparator, significantly reducing the dependence of timing information on signal amplitude. The design methodology is supported by extensive schematic-level and post-layout simulations, including parasitic extraction, Monte Carlo analysis, and transient noise simulations, to assess the performance of the ASIC in terms of noise, linearity, timing jitter, power consumption, and robustness against process variations. A dedicated acquisition system, composed of custom-designed carrier and main boards, was developed to enable full electrical characterization of the MAGIC ASIC, including biasing, configuration, and readout. The experimental setup and measurement are described, providing the framework for the experimental validation of the proposed architecture. In parallel with the main research activity, this dissertation also presents the redesign and experimental characterization of MIRA, a pixelated readout ASIC implemented in 65 nm and developed for photon-counting applications. This side project focuses on addressing scalability limitations observed in a first-generation prototype, particularly those related to static power consumption and power distribution in large pixel matrices. The redesign introduces a low-power analog front-end, an improved summing stage, and a grid-based power distribution network complemented by an adaptive biasing technique, enabling reliable operation of large-scale arrays. The experimental results confirmthe effectiveness of the proposed solutions in improving uniformity, noise performance, and robustness against supply voltage drops. Overall, this work contributes to two complementary readout architectures targeting different detector paradigms, demonstrating scalable and robust solutions for high-performance radiation detection systems. The results represent a step forward toward advanced front-end electronics for TOF-PET range monitoring in hadrontherapy and large-area photon-counting detectors.

**PhD Committee**

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