Ph.D. in Information Technology
Thesis Defense

July 13th, 2026
At 8:30 a.m.
Room Schiavoni - Building 20A

Michele ROSSONI – XXXVIII Cycle

DESIGN OF LOW-NOISE FRACTIONAL-N DIGITAL PLLS BASED ON DIGITALLY-ASSISTED ANALOG CIRCUITS
Supervisor: Prof. Andrea Leonardo Lacaita

Abstract:

The rapid advancements in CPU and GPU computing power over the last decade have driven the electronics engineering community to develop novel solutions capable of providing high-speed, reliable, and power-efficient wired data links, in order to sustain the unprecedented growth in data processing capabilities. A similar trend has emerged in the wireless domain, where the number of connected devices has grown exponentially in recent years. This expansion has introduced comparable challenges in wireless data transmission, requiring innovative architectures and circuit techniques to support the increasing demand for higher data rates, improved spectral efficiency, and reduced power consumption. Despite their different nature, both wired and wireless Transceivers (TRXs) share similar Key Performance Indicators (KPIs) that shaped their design in the last decade: - Compact area utilization in order to reduce the cost of the integrated circuit (IC) and enable integration of a large number of TRXs to support Multi Input Multi Output (MIMO) communication and Phased Arrays. - Low power consumption in order to increase the usage of battery powered devices in wireless scenarios, and relax thermal management requirements of large scale data-centers in wired applications. - Capability of supporting high-bitrate modulations to satisfy the ever-growing demand of larger data-rates posed by the increasing number of users and processing power. In order to support these KPIs simultaneously, modern TRXs are typically implemented in scaled CMOS technologies, where integration of complex digital processing is feasible with low power consumption and area occupation, and wideband modulations capabilities are achievable thanks to fast and power-efficient Digital-to-Analog (DAC) and Analog-to-Digital (ADC) Converters. However, the adoption of scaled CMOS technologies has posed several challenges in the implementation of TRX circuital components. As a matter of fact, while scaled CMOS provides better transistors for digital circuits, the analog performances of these has been sacrificed, with reduced voltage headroom, larger flicker noise, and worsened matching. For these reasons, in the last years the traditional analog design of TRX's blocks has been converted to a mixed-signal one, where analog and digital circuits operate in symbiosis to push the performance levels. In this framework, the design of TRX frequency synthesizers, adopted to up-convert and down-convert the information and provide clock signals to other TRX blocks, has observed a similar evolution, with the development of Digital Phase-Locked-Loops (D-PLLs). In this thesis, the design of high performances analog circuits has been combined with dedicated digital calibrations to compensate for their non-idealities introduced by the scaled

CMOS technology. This enabled the realization of D-PLLs with an unprecedented level of performances for scaled technologies, together with a compact area and an high integration level.

Michele ROCCO – XXXVIII Cycle

HIGH-SPEED PIPELINED-SAR HYBRID A/D CONVERTERS
Supervisor: Prof. Carlo Samori

Abstract:

In the recent years, the demand of communications with higher data rates, increased connectivity and lower latency has led to significant advancements in wireless technologies, most notably the deployment of the fifth-generation mobile network (5G) and the development of next-generation wireless standards such as Wi-Fi 7 (IEEE 802.11be). The support for wider channel bandwidths (up to 320MHz in Wi-Fi 7 and 400MHz in 5G FR2), higher-order modulation schemes such as 4096-QAM, and advanced multiantenna configurations for massive MIMO operation pose significant challenges in the design of the integrated circuits in radio links. Analog-to-digital converters (ADCs) play a crucial role in the receiver chain as they bridge the gap between the analog world with the digital one, while achieving giga-hertz sampling rate with sufficiently high resolution and linearity to support next-generation standard requirements. This Ph.D. thesis covers the concept, modeling and practical design of a digitally-assisted time-interleaved (TI) ADC, where the pipeline-SAR hybrid is the architecture of choice for the slice, simultaneously offering higher conversion speed and higher energy efficiency than conventional SAR and 1-bit pipelined ADCs, respectively. However, residue amplification is critical in pipelined ADCs and limits the achievable SNR due to residue amplifier nonlinearities and gain mismatches. Furthermore, time-interleaving limits the overall resolution due to sub-ADC mismatches, channel interactions, and the switched front-end load. This thesis presents analog and digital techniques to overcome these limitations, leading to an energy-efficient 2-GS/s, 4×-TI pipeline-SAR ADC in a 28-nm CMOS technology with 10 equivalent bits of resolution and a high-frequency spurious-free dynamic range (SFDR) higher than 75 dBc.

Gabriele ZANOLETTI – XXXVIII Cycle

ENERGY-EFFICIENT SCALING-COMPATIBLE AMPLIFIERS FOR NEXT-GENERATION A/D CONVERTERS
Supervisor: Prof. Andrea Giovanni Bonfanti

Abstract:

Analog-to-digital converters (ADCs) are an essential part of every signal chain. Batterypowered IoT and wireless applications push ADC requirements toward higher bandwidth (tens to hundreds of MHz) and better power efficiency (<10 fJ/conversion−step), while technology scaling imposes low

supply voltages, which challenge traditional analog tzchniques. A promising approach to address these challenges is the adoption of hybrid ADC architectures, such as noise-shaping SAR and pipeline-SAR converters, built upon and co-designed with low-power dynamic amplifiers. Among these, the Floating-Inverter Amplifier (FIA) stands out as one of the most promising solutions thanks to its excellent energy efficiency and scalability. Due to its high gain and simple structure, the FIA represents an ideal candidate as a building block for advanced amplifier topologies. This thesis provides new analytical insights into dynamic amplifiers and introduces three novel FIA-based topologies: • The Ratio-Based Floating Inverter Amplifier (RBFIA), an open-loop structure with improved PVT robustness compared to the standard FIA. In the RBFIA, the gain is set by the ratio of easily controllable elements. • The Current-Feedback Ratio-Based FIA (CFRBFIA), an evolution of the RBFIA that enables higher bandwidth through the use of minimum channel-length transistors. The CFRBFIA introduces a feedback that suppresses the impact of the low intrinsic gain devices by putting their output impedance to virtual ground. • The 3×-Cascode FIA, a closed-loop amplifier that achieves high gain through cascoding. The stacking of many transistors (six devices total) is possible despite low supply voltage (≈ 1 V) thanks to the proposed virtual supply extension technique. This approach employs capacitors pre-charged to the supply voltage during the reset phase to introduce voltage shifts, extending the effective voltage range. The high gain achieved through cascoding enables the use of a single-stage amplifier, relaxing the conventional trade-off between stability and bandwidth of multi-stage amplifiers, as no secondary high-impedance nodes are present. The proposed concepts are validated through simulations and measurements in a 28-nm CMOS technology. A prototype Noise-Shaping SAR ADC is presented as a demonstrator for the proposed techniques, showcasing the potential of combining architectural (a novel loop filter architecture based on the use of a multi-input amplifier and comparator) and circuit-level (the RBFIA topology) innovations. The prototype achieves 12.3 ENOB in a 20-MHz bandwidth with a Schreier FoM of 177 dB, nearly 4 dB better than comparable designs, while maintaining robust PVT performance without calibration.

Simone ZAFFIN – XXXVII Cycle

HYBRID RESONANT DC–DC CONVERTERS: DESIGN, MODELING, AND OPTIMIZATION OF DUAL-PATH AND SIGMA ARCHITECTURES
Supervisor: Prof. Salvatore Levantino

Abstract:

AS the demand for high power density and high efficiency in lowvoltage power delivery continues to grow, conventional step-down DC–DC converters face fundamental limitations in balancing conversion ratio, thermal constraints, and magnetic component size. This thesis investigates and develops advanced hybrid converter architectures that overcome the intrinsic limitations of conventional buck and switched-capacitor topologies. The work begins with a systematic analysis of the fundamental DC–DC converter families, identifying the critical bottlenecks that limit currenthandling capability, efficiency, and power density in high-current, lowvoltage applications. Building on this analysis, the concept of dual-path conversion is introduced and characterized. By distributing the load current between inductive and capacitive energy transfer paths, dual-path architectures reduce the dc current stress on the magnetic component and improve the overall power density of the converter. The primary contribution of this work is the derivation and experimental

validation of a Resonant Dual-Path Interleaved (RDPI) topology. By combining resonant soft charging of the flying capacitors with interleaved dual-path operation, the proposed architecture simultaneously achieves a reduction of the average inductor current, a minimization of the input RMS current, and the elimination of hard-charging losses. A modular averaged small-signal model of the converter is derived, enabling systematic design of the compensation network and accurate prediction of the closed-loop dynamic behavior. The proposed topology is implemented in a 0.18 μm I BCD technology co-designed with a PCB interposer that exploits shaped copper trace parasitics to realize the resonant inductance. The prototype delivers up to 7 A over a 0.75–1.2 V output voltage range from a 4.0–5.0 V input, achieving a peak efficiency of 91.6% and a peak power density of 0.5 W/mm². To address the limited input voltage range of resonant switched-capacitor converters, this thesis further introduces a sigma-regulated switched tank converter topology for 48 V-to-12 V intermediate bus conversion. The proposed architecture combines a fixed-ratio resonant stage with an auxiliary inductor-based converter operating on a reduced voltage domain, enabling continuous output voltage regulation while preserving the high efficiency of resonant energy transfer across a wide input voltage range. A prototype implemented on a discrete PCB delivers up to 60 A at 12 V with a peak power density of approximately 900 W/in³, validating the proposed architecture across the full 38–60 V input voltage range. Collectively, the architectures and analytical models presented in this thesis advance the state of the art in hybrid step-down power conversion, providing validated design methodologies for high-efficiency, high-density power delivery in both low-voltage and intermediate bus applications.

PhD Committee

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