Ph.D. in Information Technology
Thesis Defense

April 28th, 2026
At 3:30 p.m.
Entrance Room – Building 30

Emanuele SACCHI – XXXVIII Cycle

CHIPLET-BASED APPROACH TO REAL-TIME CONTROL OF PROGRAMMABLE PHOTONIC CIRCUITS
Supervisor: Prof. Giorgio Ferrari

Abstract:

There has been growing interest in recent years in the field of programmable photonic integrated circuits (PICs), as they allow the implementation, directly in the optical domain, of arbitrary linear transformations. The main advantage of transmitting and processing information by means of photonic devices, either discrete or integrated, resides in the extended bandwidth, minimal cross-talk and reduced power dissipation associated with light based communications. On top of that, the possibility of fabricating PICs on a Silicon Photonics platform, which uses the same process steps adopted for the CMOS technology, indeed improves the overall rentability of optical integrated systems. A PIC only becomes programmable if it is provided with an electronic control layer that reconfigures its devices according to the desired functionality by driving actuators that properly manipu late the propagation of the optical signal. The scope of this layer is twofold: it has both to configure the correct working point of each actuator and to stabilize it over time against any fluctuation that may affect the optical link, either concerning the PIC itself (e.g. thermal drifts) or the phase of the propagating wavefront. This latter requirement also advocates for the definition of a closed-loop system, able to dynamically track the desired PIC configuration. Several solutions have already been proposed for real-time control of photonic integrated circuits. Yet, as PICs scale in complexity, now featuring tens or even hundreds of devices to be configured simultaneously, a quest opens up for the definition of electronic controller architectures that can keep up with the pace of photonics in terms of area occupation and power consumption. In this thesis, a chiplet-based approach to the problem of real time control of programmable PICs is proposed. The fundamental idea behind this project is that, given the integrated, CMOS based nature of Silicon Photonics processors, the dedicated control electronics should be fabricated on an integrated platform as well, possibly with as small impact as possible on the overall system in terms of bulkiness and energy demand. After the introduction and a discussion about the general architecture of the overall electrical-optical system, 2 different mixed-signal application specific integrated circuits (ASICs) will be presented. The first one, fabricated in 2023 in a 350nm CMOS technology node, successfully allowed to establish up to 50Gbit/s optical free-space links, proving capable of dynamically reconfiguring the photonic processor to compensate injected turbulence. After several proofs of concept validating the chiplet-like approach, in 2025 a second chip was fabricated in a more scaled technology node (180nm), which allowed the assembly of the ASIC-PIC system in a compact flip-chip arrangement. Here, the massive adoption of digital electronics to implement the control algorithm allowed to further shrink the

footprint of the circuitry and reduce its power consumption, thanks to the design of oversampling converters and PWM-based actuators, ultimately paving the way to the design of seamlessly scalable architectures.

PhD Committee

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