

**Ph.D. in Information Technology
Thesis Defense**

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ADVANCED RELIABILITY ISSUES IN 3D NAND FLASH MEMORIES

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Abstract:

The Flash memory technology has conquered the non-volatile memory market few decades ago when it has reached the reliability and the storage capability of the magnetic memories. In particular the NAND Flash memory represents a very low cost solution while it has a huge potential in terms of operation data throughput. The evolution of the 2D NAND Flash memory kept going on at an impressive pace reaching a bit-storage density incredibly high. The scaling process of the planar geometry reached a so advanced miniaturization that the single cell started to manifest fundamental issues related to the limitations of the physics involved in the device operation. In order to avoid these problems and continue the process of developing devices with a higher integration density, a paradigm change of the manufacturing process was necessary. The process of shrinking the planar dimension of the single cell was replaced with the process of stacking memory arrays one above each other along the direction perpendicular to the wafer plane. In such a way, a three-dimensional structure that could mitigate the constraints on the minimum dimension of the memory cell was developed. So, the 3D NAND Flash technology was born and, essentially, it is mainly composed by a set of vertical channels surrounded by a stack of alternated layers of insulating materials and conductive electrodes. This change in the geometry brought an improvement of the memory reliability but, at the same time, gave birth to new relevant issues due to both process and geometry constraints. For instance, the substrate where the conduction channel is established is made of polysilicon. This feature increased the variability of the memory cells and, at the same time, played a relevant role at modifying the cell transcharacteristic. Furthermore, the well known reliability issues, such as the Random Telegraph Noise (RTN), showed new dependencies on temperature and other fundamental parameters. This was mainly due to the new fabrication processes and the presence of grain boundaries in the polysilicon channel. Some other issues are related to the lack of the body contact that, instead, was present in the planar structure. Due to this constraint, the potential of the channel is not so easily controllable and new bias settings are needed to guarantee the correct device working capability and avoid new issues, such as the Down-Coupling Phenomenon (DCP).

In such context, the present work aims to supply a thorough investigation of the relevant issues that still concern the correct functioning of the 3D NAND Flash memories. In particular, an innovative analysis of the RTN, showed by the cells of this technology, will be described. In detail, the dependence of the RTN with respect to the temperature that the device withstand during the idle periods will be analyzed. The physical picture explaining the observed results will be proposed and, in particular, the results will be described in terms of a depassivation of the defects in the polysilicon channel of the vertical NAND strings. Together with the experimental analysis, the simulations

results supporting the physical picture, presented to explain the depassivation of the polysilicon channel, will be shown. Moreover, the effects of the depassivation on the conduction mechanisms will be described and analyzed with respect to the various working conditions of the cells. In the end, a first approach for the quantification of the depassivation will be presented and described in detail.

This work, other than analyze the RTN and the polysilicon depassivation, will also report an extended description of the simulations that were carried out in parallel to the experimental work in order to analyze other kinds of issues. In particular, the simulations on the DCP will be described. This reliability issue was investigated directly through TCAD simulations and the results brought the necessary information for the development of suited countermeasures that should be implemented in the following technological nodes. In the detail, the dependences between the transient time, needed by the channel to go back to the potential equilibrium condition, and the various generation/recombination phenomena, that take place in the channel, will be analyzed. Moreover, the dependences of the phenomenon on the memory architecture will be studied. The TCAD simulations focused also on the effects of the discrete polysilicon traps on the percolative conductivity of the strings. These results will present the importance of implementing discrete traps within the polysilicon channel. Since this discrete definition, with respect to the continuous definition, will be shown to affect significantly both the cell V_T and the RTN.

Finally, with the technology evolution, the memory devices have been used in many different working conditions such that their structural characteristics were designed to fit the environment requirements. In this framework, the quantum computing development requested the exploitation of memory devices at very low temperatures, very close to the absolute zero. Within this perspective, the behavior of the 3D NAND Flash memories is analyzed at cryogenic temperature in order to evaluate their characteristics in this temperature regime and confirm the possible integration of this technology in the circuits that control the quantum processors. With such goal, in this work the investigation of the behavior of this technology in such a harsh environment focused on the analysis of the conductivity of the polysilicon channel and the drift of the threshold voltage of the cells as a function of the temperature within the cryogenic regime. The new conduction characteristics of the string will be presented and an innovative interpretation of the phenomenon will be given. In detail, the negative conductivity of the cells will be associated to a SET-like conduction mechanism. This conduction mechanism has been exploited considering the presence of localized potential wells originated by the defects present within the polysilicon grain boundaries. This analysis will give important information on the path to cover in order to stabilize the properties of the technology at cryogenic temperatures and allow the exploitation of the 3D NAND Flash memories in the quantum computing systems.

PhD Committee

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