Ph.D. in Information Technology
Thesis Defenses

January 25th, 2022
at 9:00
online by Teams

Giulio FRANCHINI – XXXIV Cycle

Characterization and modeling of current transport and polarization switching in FTJs

Supervisor: Prof. **Alessandro Sottocornola Spinelli**

Abstract:

In the last decades PCs, smartphones and wearable and interconnected electronic gadgets are gaining more and more momentum. Due to this large success, the memory sector experienced an enormous growth. Memories underwent an intensive scaling process to reduce the cost for stored bit and encountered huge reliability issues. Moreover, the performance gap between the central processing unit (CPU) and the working memory (DRAM) has never stopped growing in the last forty years. This gap results in a memory bottleneck that reduce the overall performance of a computing system. The aforementioned issues fuelled the research on novel memory technologies, both volatile and non-volatile, different from the ones that dominate the market. This work focuses on one of the promising candidates, Ferroelectric Tunnel Junction (FTJ). In particular, an experimental characterization on FTJ samples has been carried out, exploring the main features of the device: resistive window, retention, I-V characteristics. Experimental activities are followed by the development of a one-dimensional in-house MATLAB code for the device simulation, capable of reproducing the I-V characteristics and explaining some of the physical phenomena involved. Therefore, efforts have been directed toward the analysis of the switching process, a two-dimensional switching simulator has been developed and integrated with mono-dimensional one. The obtained results are promising and this simulator can undoubtedly be of help in better understanding physical phenomena involved during ferroelectric switching in FTJs.

Mauro LEONCINI – XXXIV Cycle

Time-based controller for DCDC boost converter with right-half-plane zero mitigation

Supervisor: Prof. **Salvatore Levantino**

Abstract:

TIME-BASED controls in integrated wide-band DC/DC buck converters for smart power applications have been proven to reduce area occupation and power consumption of the controller with respect to the standard voltage-mode signal processing since they operate with digital signals. The time-based approach applied to a boost converter only gives limited advantages since, the latter, suffers

from an inherently right-half- plane zero in the control loop that limits the maximum achievable bandwidth. The aim of this project is to develop a novel time-based controller architecture for boost DCDC converter that can increase the maximum achievable bandwidth, eliminating the right-half-plane zero in the control loop, thus fully exploiting the advantages given by the time-based architecture. A time-based boost converter for LED display applications is presented. The controller combines the converter output voltage with the inductor current to eliminate the RHP zero and improve the dynamic performance without any extra power switches or external capacitors. The steady-state regulation error generated by this technique is mitigated by injecting a scaled version of the load current into the loop. The efficiency at light-loads is increased thanks to a PFM operating mode with a steady-state error correction and seamless PFM-to-CCM transition. The prototype boost converter implemented in a 0.18µm BCD process generates an output voltage of 5V when powered by a Li-ion battery providing an input voltage varying from 2.5V to 4.5V. The converter peak efficiency is 96% for an input voltage of 4.5V and above 90% at light-loads up to 10mA. The proposed time-based controller shows a quiescent current of 300µA when operating in CCM and an area occupation of 0.27mm2, with 0.12mm2, 0.04mm2, and 0.11mm2 being the occupation of the compensator, inductor current sensor, and load current sensor, respectively. The prototype converter shows an increase in the converter bandwidth of about a factor 5 with respect to a standard compensation limited by the RHP zero while reducing the worst-case static error from 120mV to 10mV, thanks to the addition of the novel static error correction.

Angelo PARISI – XXXIV Cycle

Digitally assisted frequency synthesizers and data converters for wide-band radio systems

Supervisor: Prof. **Andrea Lacaita**

Abstract:

Technology scaling has been driving integrated circuits designers towards denser and faster systems since its early days, in turn influenced by the increasing demand of performance. Main protagonists of the revolution are communication systems, which currently adopt RF and mm-Wave carriers for high throughput data transmissions requiring modulation bandwidths ranging from few hundred MHz to about 1GHz. State- of-the-Art radios must then reach unprecedented accuracy on wide ranges of frequencies and operating conditions, at the same time coping with the worsened analog performance of the high-density, digital-friendly technologies allowing to reach such frequencies. The change in paradigm of recent years, favouring digital assistance of the essential analog building blocks, blurs the edges of mixed-signal implementations: the cost and overhead of ppm accuracy of analog designs is circumvented by means of digital calibrations, steering towards systems that minimize the amount of custom building blocks preferring scalable, reusable and portable subsystems. Examples of this trend are frequency synthesizers and data converters, cores of most radios.

In this work are presented examples of designs that might enable efficient new generation radios, starting from digital and hybrid 13GHz Phase-Locked Loops, embedding high efficiency oscillators to achieve sub-100fs r.m.s. jitter with low power consumption, to GSps time-interleaved Analog-to-Digital converters combining several low-power cores controlled by digital background correction algorithms reducing spur power to less than 70dB below the carrier. Efficiency and performance are

achieved by means of novel Least Mean Squares control loops and adaptive filters for distortion and mismatch compensation.

PhD Committee
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