Ph.D. in Information Technology: Thesis Defense

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online by Teams – at 10.00

Saleh KARMAN – XXXIII Cycle

Multi-Core Frequency Synthesizers for mm-Wave Communications

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Abstract:

This work proposes multi-core frequency synthesizers as a promising architecture for the synthesis of low-noise mm-Wave carriers. Multi-core PLLs, similarly to multi-core oscillators, leverage coupling between several cores to exploit the noise-power trade-off and achieve very low integrated jitter levels. The potentialities of this architecture are phase-noise reduction (both inside and outside the PLL's bandwidth), an overall simplification of the design with respect to multi-core oscillators-based architectures, and the possibility to couple an arbitrary number of cores. Two different architectures will be discussed and compared to synthesize a low noise carrier: PLLs with filter coupling and PLLs with output signal combination. A prototype of a 20GHz dual-core PLL based on the power-combining architecture was designed and implemented in a 55nm-BiCMOS technology. The test-chip, featuring a dual-core architecture, including an offset correction loop and an efficient second harmonic extraction scheme, exhibits an integral jitter of 206fs-rms and 174fs-rms consuming 18 and 42.6mW in the single-core and dual-core configurations, respectively. The achieved results allowed to match, with two PLL cores only, the spot noise of the best quad-core oscillator realization published in the same technology, with the same power consumption and minor area overhead.

PhD Committee
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