

Ph.D. in Information Technology: Thesis Defenses

February 6th, 2020

Conference Room "E. Gatti" – 2.30 pm

Elia AMBROSI – XXXII Cycle

“Characterization of Resistive Switching Devices for Memory and Computing”

Advisor: Prof. **Daniele Ielmini**

Abstract:

Approaching the end of Moore’s law, the advancement of CMOS technology is reaching a plateau. In addition, computing performance is nowadays limited by the memory wall, with most of the computing time spent in shuttling data between the processor and the memory. Emerging memory technologies promise to tackle these obstacles by complementing the memory hierarchy with massive amount of non-volatile memory fabricated on the CMOS chip. Moreover, they enable novel computing paradigms, such as in-memory computing and neuromorphic computing, where memory and logic functions are distributed within the same network. Resistive switching memory (RRAM) is one of the most promising emerging technologies, thanks to its excellent scalability, high writing speed, good endurance, low fabrication cost and good compatibility with the back-end-of-line of standard CMOS process. However, RRAM faces serious reliability issues due to programming variability and resistance fluctuations over time, which prevent its adoption as a commercial technology. This Doctoral Dissertation focuses on the characterization of RRAM devices for high-density crosspoint arrays, and on their application in novel in-memory computing systems. First, novel memory and selector devices based on a silicon oxide (SiO_x) technology are presented and studied from the point of view of the switching characteristics. The non-volatile memory is then compared with a HfO₂-based RRAM technology, at fixed electrode materials and device geometry, to investigate the material parameters driving device performance and reliability. Subsequently, an extensive reliability study of the non-volatile SiO_x-based RRAM is carried out to enable low-current operation in high-density memory array. The last part of the Dissertation focuses on the RRAM applications in digital and analogue computing. First, a neural network-based reconfigurable RRAM circuit is implemented, and several logic functions, along with a 1-bit full adder, are experimentally demonstrated. Then, incremental programming techniques are investigated to achieve gradual set and reset operations, enabling a controllable tuning of the RRAM conductance. RRAM devices are arranged into a crosspoint circuit to perform analogue computations within the memory.

Roberto CARBONI – XXXII Cycle

“Characterization and modeling of spin-transfer torque (STT) magnetic memory for computing applications”

Advisor: Prof. **Daniele Ielmini**

Abstract:

With the ubiquitous diffusion of mobile computing and Internet of Things (IoT), the amount of data exchanged and processed over the internet is increasing every day. For the past 50 years, microelectronics has evolved according to Moore’s Law, which describes the exponential growth of the number of transistors on integrated circuits (IC). Such trend is now slowing down due to the increasing heat dissipation and the growing impact of charge/dopants discretization on device performances. In addition, von Neumann architecture-based digital processors are hindered by the performance gap between the central processing unit (CPU) and memory, which makes them generally inefficient in terms of both energy and latency particularly in data-centric applications such as machine learning. To face such challenges, emerging memory technologies, such as resistive switching random access memory (RRAM), phase change memory (PCM), ferroelectric memory (FERAM) and spin-transfer torque magnetic memory (STT-MRAM) have been proposed as solutions thanks to their non-volatility, area scalability, low current and fast operation, and compatibility with the CMOS process. Moreover, various approaches to overcome the von Neumann bottleneck, such as stochastic and neuromorphic computing, are under intense scrutiny by both academia and industry. In this regard, in addition to enabling improved memory performances, STT-MRAM peculiar stochastic switching variability has drawn considerable attention since it can be exploited for the emulation of brain-inspired spiking behavior. This doctoral dissertation deals with the experimental characterization and modeling of the conduction, switching and reliability of STT-MRAM. On the one hand, this effort aims to understand the limitations of STT-MRAM in terms of breakdown-limited cycling endurance and stochastic switching towards an implementation of STT-based memory circuits. On the other hand, the proposed compact models allow for the exploration of possible applications of STT-MRAM as hardware primitive for security and computing.

Giacomo PEDRETTI – XXXII Cycle

“In-memory computing with memristive devices”

Advisor: Prof. **Daniele Ielmini**

Abstract:

Microelectronics industry has been driven by the Moore’s Law in the last decades, which led to robust cooperation between technologist, architects and packaging engineers to exponentially increase the performance of microprocessor, every couple of year. Unfortunately, many issues are

tackling the mirage of eternal performance growth. Modern chips need to slow down their clock speed to control their intensive heating during computation and protect themselves from damage. Large amount of energy is spent for moving data from the memory to the processor in conventional Von-Neumann architectures, resulting in a bottleneck for the data intensive era, which requires many memory accesses, dictated by the communication. To overcome these challenges, from one side new low-energy nanoscale devices are desired, from the other unconventional efficient architectures are needed.

Merging novel in-memory, brain inspired and specialized architectures with nanoelectronics emerging memories is the goal of this Ph.D. dissertation. Different computing paradigms, namely spiking neural networks and analog computing, have been explored and networks based on different emerging memories have been realized, demonstrating in hardware new computing concepts.

PhD Committee:

Prof. **Christian Monzio Compagnoni**, DEIB

Prof. **Fabrizio Bonani**, Politecnico di Torino

Prof. **Paolo Pavan**, Universita' di Modena e Reggio Emilia