Ph.D. in Information Technology: Thesis Defenses

February 3rd, 2020

Room Conferenze "E. Gatti" – 10.30 am

Luca BERTULESSI – XXXI Cycle

"Frequency Synthesizers based on PLLs for Cellular Radio Applications"

Advisor: Prof. **Salvatore Levantino**

Abstract:

New 5G communication standards have to cover different frequency ranges to face the increasing demand of high data rate wireless access and the growing number of devices simultaneously connected to the network. Therefore, the 5G radio devices need to exploit also a new spectrum segment above 30GHz in the so-called mm-wave range in addition to the legacy sub-6GHz segments. Due to the narrow channel spacing and the crowded spectrum segment, sub-6GHz devices have to meet stringent phase noise masks while in a mm-Wave device, due the high output frequency, low jitter is mandatory to guarantee the bit error rate (BER) required by the specifications. The target of this PhD thesis is to identify which phase locked loop (PLL) and oscillator architectures are the best candidates to reduce the output phase noise and satisfy the 5G stringent specifications in both frequency ranges. For sub-6GHz PLL the analysis faces the trade-off between phase noise and the power consumption. The energy efficiency of CMOS LC oscillators is discussed, and the best topology to meet the out-of-band phase noise mask, without increasing too much the power consumption, is identified. The adoption of a digital PLL architecture based on a single bit phase detector (bang-bang) reduces the power consumption but exacerbates the trade-off between bandwidth and locking transient. In this PhD thesis a novel technique based on nested DCO control loops is presented, thus speeding-up locking transient in bang-bang digital PLLs. The implemented sub-6GHz fractional-N synthesizer in 65nm CMOS technology has an output frequency from 3.59GHz to 4.05GHz with an integrated output jitter of 182fs. Fractional spurs are below −50dBc and the system has a power consumption of 5.28mW from 1.2V power supply leading to a FoM of −247.5dB. Thanks to the implemented locking technique the loop can perform a frequency step of 364MHz, to within 10 MHz from the final frequency, in only 5.6µs. These figures advance the state of the art in terms of power-jitter FoM and locking time of a digital PLL. The challenging mm-wave targets were instead defined to push performance, thus reducing the existing gap with respect to the sub-6GHz synthesizer. A new sub-sampling bang-bang phase detector topology has been investigated. A low-power divider-by-six prescaler has been adopted in the feedback path to reduce the overall power consumption. The resulting implemented synthesizer, in 65nm CMOS technology, can operate in the mm-Wave range between 30.4 and 34.2 GHz with an integrated RMS jitter below 180 and 197.6 fs for the integer-N and fractional-N channels, respectively. The fractional spurs, measured at the 5-GHz prescaler output, are below −54 dBc, even considering near-integer channels. The power

dissipation of 35 mW from the 1.2-V supply leads to a −238.6 dB jitter-power figure of merit for fractional-N channels that advances the state of the art in terms of power-jitter FoM.

Mario MERCANDELLI – XXXII Cycle

"Techniques for Low-Jitter and Low-Area Occupation Fractional-N Frequency Synthesis"

Advisor: Prof. **Salvatore Levantino**

Abstract:

In the last decades, wireless connected mobile devices became pervasive in the consumer market, thanks to the constantly increasing datarate capability and power efficiency offered by modern transceivers. To enable higher communication bandwidth and reduce the transceiver cost, the frequency synthesizer implementing the transceiver local oscillator (LO) has to operate under stringent low output jitter requirements, with low area occupation and integrated in the same CMOS technology as the digital baseband processor.

In this thesis, two viable alternatives to meet these stringent requirements are presented.

First, an extremely low-jitter and low area occupation frequency synthesizer is presented, based on a sampling type-I analog PLL, which avoids the large integrating loop-filter capacitance of type-II analog PLLs. To suppress the phase detector (PD) noise contribution and achieve a low reference spur, a high-gain sampling PD is used.

Recently published sampling type-I PLLs are bounded to integer-N operation, due to the phase detector narrow-range. Fractional-N operation is enabled by canceling the quantization noise before the phase comparison. The proposed sampling type-I PLL has been fabricated in a 28nm bulk CMOS technology process. The measured RMS integrated jitter is 58.2 fs around a 12.5 GHz carrier, with a reference spur as low as -73.5dBc and fractional spurs lower than -63.2dBc. With a power consumption of 18mW, the achieved figure-of-merit (FoM) is -252dB, outperforming recent fractional-N frequency synthesizers. Thanks to the type-I architecture and the proposed digital algorithms, the area occupation is only 0.16mm2.

Second, an attractive alternative for the frequency synthesizer implementation is presented, which relies on a fractional-N digital PLL. Area occupation and power consumption are reduced by relying on a 1-bit time-to-digital converter and a digital loop filter. Extensive use of digital adaptive algorithm is leveraged, and a technique to accurately control the PLL bandwidth, desensitizing the loop gain from any analog dependence, is proposed. The digital bang-bang PLL has been fabricated

in a 65nm CMOS process, occupying a core area of 0.22mm2, with a 400fs RMS jitter around a 3.6GHz carrier. The PLL bandwidth is controlled with an accuracy better than 4%.

Alessio SANTICCIOLI – XXXII Cycle

"High-Efficiency Inductorless Frequency Synthesis"

Advisor: Prof. **Salvatore Levantino**

Abstract:

The roaring demand for wireless connectivity at a low price point has, in recent years, spurred the interest for highly-integrated transceiver solutions able to cut down on expensive silicon area requirements. In this context, one of the major limiting factors is generally represented by the frequency synthesizer used to generate the local oscillator signal for the transceiver. Conventionally implemented as phase-locked loops (PLLs) based around LC-oscillators, they require large amounts of area due to their use of integrated inductors, that additionally do not benefit from process scaling. However, they are generally preferred to ring-oscillator-based solutions, as they offer a superior jitter-vs-power tradeoff, which benefits the overall transceiver efficiency. A promising alternative to LC-based PLLs, which overcomes the efficiency limitations of conventional inductorless implementations, is represented by the recently proposed multiplying delay-locked loop (MDLL) architecture. Leveraging injection-locking, these kinds of systems provide aggressive filtering for ring-oscillator phase noise, ensuring both low-jitter and low-power operation in the integer-N mode. Unfortunately, when extended to fractional-N frequency synthesis, MDLLs suffer from a large jitter penalty due to the noise introduced by the digital-to-time converter (DTC), which is required to perform edge-synchronization. This, in turn, leads to a substantial performance gap between the integer- and the fractional-N mode, which prevents their use in demanding applications. This work aims at closing the performance gap, by proposing a number of design methods and techniques to improve the jitter-power tradeoff of fractional-N MDLLs. First, an accurate time-variant model for MDLL phase noise is developed and analyzed to derive close-form expressions for the output spectrum. Then, leveraging the results obtained from this model, the MDLL jitter-power tradeoff is examined and conditions for optimum performance are identified. Finally, the DTC design tradeoffs are evaluated and a technique to significantly reduce its jitter contribution is proposed. To validate these results, a fractional-N MDLL has been fabricated in 65nm CMOS (Fig. 1). The prototype

occupies a core area of 0.0275 mm2 and draws 2.5 mW power from a 1.2 V supply. The maximum RMS jitter is 334 and 397 fs for the integer-N and the fractional-N case, respectively. Achieving a jitter-power figure-of-merit (FoM) of -244 dB in the fractional-N mode, the proposed system effectively bridges the gap to integer-N implementations.

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