Ph.D. in Information Technology: Thesis Defenses

July 26th, 2019

Room Seminari – 11.00 am

Michele GIORGIO – XXXI Cycle

"High Resolution Direct-Written Field-Effect Transistors for High-Frequency Applications"

Advisor: Prof. **Marco Sampietro**

Abstract:

In this thesis work, we resorted to Scattering parameters (S-parameters) for reliable determination of the frequency of transition without extrapolations. We report n-type FETs based on a solution-processed polymer semiconductor where the critical features have been realized by a large-area compatible direct-writing technique, allowing to obtain record frequencies of transition of 19 MHz in the case of n-type and 24 MHz for p-type polymer transistors. This is the first report of solution-processed organic FETs characterized with S-Parameters. We then made a step forward in the improvement of the OFETs maximum operational frequency by reducing the gate to source and gate to drain geometrical overlap to some hundreds of nanometers by fabricating also the gate contact by laser sintering. In this way we succeeded in the demonstration of the fastest n- and p-type organic transistors ever realized, showing transition frequency of 70 MHz and 100 MHz, respectively. Finally, in order to fabricate high-performance organic circuitry, we propose a method for self-assembled monolayers (SAMs) formation by using inkjet printing techniques, allowing to grow different SAMs on the desired contacts on the same substrate. We demonstrated both n and p unipolarized devices starting from a single ambipolar semiconductor uniformly bar-coated on the substrate, with mobilities higher than 1 cm2/Vs in both cases.

Francesca SCURATTI – XXXI Cycle

"Printed Carbon Nanotubes Based Transistors: from Charge Transport Studies to Biosensing Applications"

Advisor: Prof. **Marco Sampietro**

Abstract:

This dissertation reports the investigation of charge transport dynamics in mixed networks of printed SWCNTs-based field-effect transistors and their application as cell-proliferation monitors.

Several analytical tools were employed to assess the impact of network density and functionalizing polymer on charge transport mechanisms in inkjet printed networks of polymer-wrapped nanotubes, demonstrating the possibility to tune their ambipolar behavior and their charge transport efficiency by tailoring the printing process. Subsequently, an application for such networks is proposed, introducing carbon nanotube based

electrolyte-gated transistors as a novel tool to electrically monitor in vitro cell adherence and proliferation, able to operate consistently in aqueous environment and in conjunction with more established optical techniques.

Alireza TAJFAR - XXXI Cycle

"High speed and intensity laser diode drivers for Time-of-Flight 3D ranging and Pico-Projectors"

Advisor: Prof. **Franco Zappa**

Abstract:

In the last decade, the ability to drive lasers with high frame-rate (higher than standard video-rate), with very faint illumination, has become more and more important in many fields, like ambient surveillance, road safety, identification of people and objects, biomedical imaging, studies on physics of materials as well as commercial applications such as gaming, laser-based projection and augmented virtual reality glasses. There is a growing interest in devices capable of projecting or acquiring high framerate 2D or 3D videos. This work presents the design of a 4-channel integrated laser diode driver (LDD) fabricated in 160 nm BCD technology for a low-power pico-projector application based on micro-electromechanical systems (MEMS) micro-mirrors and the design of a high-power and intensive single-chip LDD in the same technology for direct time of flight (TOF) measurement in Light Detection and Ranging (LiDAR) application. The embedded 10-bit current DAC in pico-projector LDD known as video DAC, can produce 300MHz sharp current pulses with 1ns rise/fall time, less than 7% overshoot, 3-4ns settling time while the full-scale range (FSR) is also programmable through a static 10-bit current DAC, known as scale DAC, in the range of 160uA up to 160mA. These performances are guaranteed thanks to the novel active bootstrap presented in this work. TOF LDD, as the second part of this Ph.D. thesis, can produce a fully programmable sharp current pulses up to 20A with less than 1ns duration and a repetition rate of 40MHz. to reach such high performances, a new driving topology is proposed which has brought new challenges in the design that must be mitigated by innovative solutions.

Tuan Minh VO – XXX Cycle

"A Study of High-Performance Frequency Synthesizer Based on Bang-Bang Digital Phase-Locked Loop for Wireless Applications"

Advisor: Prof. **Salvatore Levantino**

Abstract:

High-performance frequency synthesizer is a fundamental part of almost any modern wireless communication device, for example, used for coherent demodulation/modulation in wireless transceivers. The frequency synthesizer based on phase-locked loop (PLL) architecture, serving as a local oscillator in a

transceiver, is indeed a negative feedback control system generating an output signal whose frequency is multiple of the reference signal frequency. The multiple can be an integer or a fractional number. Though fractional-N PLLs entail the key advantage of a finer frequency resolution, the noise-power figure-of-merit (FoM) of state-of-the-art integer-N PLLs is still better than in the fractional-N case. In addition, digital PLL synthesizers are taking over conventional analog ones, because of their benefits in terms of power consumption and area occupation in ultra-scaled CMOS technologies. The digital solution simplifies the design and, as this is portable to the next technology nodes, may potentially reduce the time-to-market. In this study, a fractional-N digital PLL having a bang-bang (BB) phase detector with only two output levels of 1 and −1 is of interest. This topology of fractional-N digital PLL has been demonstrated in practice being able to obtain a FoM close to the best of the integer-N ones.

The objective of this study is to give an insight, for the first time, into the behavior during the transient of the fraction-al-N digital BB-PLL in two separated cases, i.e., with the frequency aid technique in the first case and with the least-mean-square (LMS) calibration loop in the second one. In order to reach this goal, analysis is carried on in the time do-main for the frequency aid technique. Based on the analyzed result, we propose a novel frequency aid technique to fur-ther improve the frequency locking speed. In the worst case of the frequency locking, the proposed technique reduces the transient time by a factor of 3.5. The LMS calibration loop is evaluated in accordance to the value of the fractional part of the frequency control word. The analysis, that is carried on in both the time-domain and the z-domain, not only gives qualitative results but also quantity results in some cases. Moreover, two novel calibration schemes are proposed to use a smaller delay range digital/time converter (DTC) while keeping a short convergence time. At the same conver-gence time, the required DTC time range in the first proposed scheme is 0.57 times, and, the one in the second proposed scheme is 0.55 times as of the ones in the conventional schemes, respectively. All of analysis is verified by simulation based on accurate behavioral models. The models are built with real design parameters, and, designed for the BB-PLLs synthesizing an output frequency from 3.2 GHz to 4.0 GHz from a reference frequency of 52 MHz.

PhD Committee:
Prof. **Marco Sampietro, DEIB**
Prof. **Piero Cosseddu**, Universita' di Cagliari
Prof. **Roberto Raiter**i, Universita' di Genova