Ph.D. in Information Technology: Thesis Defenses

February 25th, 2019

Conference Room "Emilio Gatti" – 10.30 am

Dmytro CHERNIAK - XXXI Cycle

"Digitally-intensive Frequency Modulators for mm-Wave FMCW Radars"

Advisor: Prof. **Salvatore Levantino**

Abstract:

The vast number of FMCW radar applications generates the demand for highly-linear, low-noise and reconfigurable fast chirp synthesizers implemented in high-volume deep sub-micron CMOS technologies. Conventional analog PLL-based chirp synthesizers realized in bipolar or BiCMOS technologies demonstrate an excellent phase noise performance, however, the modulation speed is typically limited by a narrow-bandwidth PLL. The emerging digital PLL-based synthesizers demonstrate prominent phase-noise and modulation-speed performance along with high degree of reconfigurability. The first part of the thesis derives the specification of the FMCW frequency synthesizer employing a new radar system model which was developed within the scope of this work. The proposed system model allows to analyze the impact of the chirp synthesizer impairments, such as phase noise and nonlinearity, on the performance of the FMCW radar system. The second part is focused on the analysis and design of two digital PLL prototypes in CMOS, which includes a novel pre-distortion scheme for DCO and DTC nonlinearity correction. The first implemented digital PLL-based FMCW modulator prototype is fabricated in 65-nm CMOS technology and demonstrates above-state-of-the-art performance of fast chirp synthesis. It is capable of maximum chirp slope of 173 MHz/µs and idle time of less than 200ns after an abrupt frequency step with no over or undershoot. The 23-GHz digital bang-bang PLL consuming 19.7 mA exhibits the phase noise of -100 dBc/Hz at 1MHz offset from the carrier and the worst case in-band fractional spur level is below -58 dBc. The second PLL prototype was developed and fabricated in 28 nm CMOS technology focusing on low-fractional spur operation. The novel digital pre-distortion scheme was applied to mitigate DTC nonlinearity in an 18-GHz digital bang-bang PLL which achieves in-band fractional spur level below -63dBc and exhibits the phase noise of -100 dBc/Hz at 1 MHz offset from the carrier.

Luigi GRIMALDI – XXXI Cycle

"Frequency Synthesizers Based on Digital PLLS for Cellular Radio Applications"

Advisor: Prof. **Salvatore Levantino**

Abstract:

Current and future mobile communication standards are targeting a new 10x increase in data rate in the following 10 years. In this context, frequency generation circuits are asked to reach lower phase noise and spur levels at lower power consumption, while operating in the range of several tenths of gigahertz. In the last few years, digitally-assisted analog design has been proven to be effective in improving performance in more scaled CMOS nodes. In this scenario, the Ph.D. thesis proved the high performance and high efficiency of frequency synthesis for wireless standards by means of digital phase locked loops (DPLL) based on single-bit phase detector (bang-bang). The validity of the proposed techniques has been assessed via fabrication of two test chips in 65 nm CMOS process, in the sub-6GHz range and in the mm-Wave range (around 30 GHz). The sub-6GHz prototype features a new digital predistortion algorithm to linearize the digital-to-time converter characteristic (DTC) and a fast lock over a wide frequency range to overcome the limited bang-bang phase detector lock range. Low power consumption of 5.28 mW, spot phase noise at 20MHz offset of -150.7dBc/Hz (which satisfies the tight GSM specifications) have been achieved. Measurements on the fast lock technique proved a recovery time of 5.6 µs to get within 10MHz from the final frequency value when a step of 364 MHz of the output frequency is performed. The mm-Wave PLL demonstrator benefits, in terms of both power and jitter, of the bang-bang phase detector used in a novel sub-sampling mode. A digital phase selection technique leads to a reduced output jitter without affecting power consumption. Low-output jitter of 197.6 fs combined with a power consumption of 35 mW makes this implementation the 1st 30 GHz digital PLL with less than 200 fs RMS integrated jitter and leads to the lowest FoM (Figure of Merit) for single loop PLLs over 24 GHz.

PhD Committee:
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