Ph.D. in Information Technology:
Mansouri Final Dissertation

Como Campus, L-NESS conference room
July 14th, 2017
10.00 am

Ph.D. presentation and discussion:

Aida MANSOURI– XXIX Cycle
"Nanofabrication and Characterization of High-Performance Graphene Field-Effect Transistors"
Advisor: Prof. **Roman Sordan**

Abstract:

The unique electrical, thermal, and physical properties of graphene have attracted research interest both from the electronics and materials science communities. Scaling limitations in conventional silicon technology, pushed the technology market to investigate new materials. Graphene, with exceptionally high mobility and being cheap, flexible, transparent and a true 2D material, gained much attention in the field of nanotechnology. Since the discovery of graphene in 2004, graphene electronics have made significant improvements. Many devices from single transistors to more complex analog and digital circuits have been demonstrated. However, along with progress, the physical limitations of graphene have become more evident.
The dominant part of this work concerns nanofabrication and characterization of graphene field effect transistors (GFETs) for high frequency applications. Using GFETs as building blocks, more complex devices were demonstrated, such as graphene inverters. During this work the main limiting factors, such as large contact resistance, high gate resistance, and poor gate oxide-graphene interface quality, which suppress the figures of merit in graphene electronic devices, were studied and characterized. Promising improvements were achieved by optimizing and adjusting process parameters. To investigate the scaling effects on intrinsic parameters of GFETs, S-parameter measurements from 10 MHz to 50 GHz were performed on various radio-frequency GFETs. A GFET small signal model was simulated and optimized to extract the intrinsic parameters. In GFETs with good saturation and transconductance, the cutoff frequency fT = 13 GHz, the maximum frequency of oscillation fmax = 27 GHz and intrinsic voltage gain Av > 30 dB for GFETs with W = 10 μm, L = 1 μm, were extracted. We believe that by passivating graphene, improving the quality of the oxide-graphene interface, and utilizing smooth and charge-trap free substrates, further improvements in graphene device performances could be achieved.

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