Ph.D. in Information Technology
Thesis Defenses

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Sala Conferenze Emilio Gatti

Lorenzo SCALETTI – XXXVI Cycle

ANALOG FRONT-END CIRCUITS FOR HIGH-RESOLUTION WIDE-BAND ADCS

Supervisor: Prof. Luca Bertulessi

Abstract:

The relentless advancement of technology, characterized by rapid evolution, ever-increasing computing power, and miniaturization, is expected to persist well into the foreseeable future. This will lead to a proliferation of electronic devices, exponentially increasing the volume of data transmitted. The trend of integrating multiple interconnected devices into everyday appliances, spanning domains from home automation and smart vehicles to wearable technologies, Industry 4.0, and smart cities, is set to significantly increase the number of connected devices, including small, energy-efficient, battery-operated embedded systems. Furthermore, emerging data-intensive applications like 8K video streaming, online gaming, video conferencing, telecommuting, and virtual reality, will drive the demand for very high throughput wireless connections. In this context, wireless networks, including the currently expanding 5G networks and the forthcoming Wi-Fi 7 (802.11be) standard, take on a pivotal role, promising enhanced data rates and reduced latency without sacrificing the energy efficiency. Modern telecommunication standards mandate high-performance Analog-to-Digital Converters (ADCs) to enable effective communication between the wireless transceivers and the digital signal processing (DSP) units. Multi-Gigabit per second links, enabled by techniques like channel aggregation and high-order modulation schemes, dictate the requirement for wide-bandwidth (>1 GHz) and medium to high-resolution (>50 dB) data converters. However, designing high-resolution ADCs in the Giga-samples per second (GS/s) range poses formidable challenges. Time interleaving emerges as a viable technique to extend the bandwidth of energy-efficient, low-frequency ADCs. However, it introduces challenges such as inter-channel mismatches (i.e., offset and gain mismatches, and sampling clock skew) and interactions, which result in spectral artifacts that degrade the effective resolution compared to single-channel ADCs. This thesis revolves around the development of a time-interleaved data converter able to meet the stringent specifications. The simple and scalable Successive Approximation Register (SAR) topology, known for its commendable energy efficiency in modern technology nodes, emerges as an optimal candidate to implement the sub-ADCs of a time-interleaved converter array. The implementation of a SAR core, optimized for speed, was therefore the first step of the research endeavor. This involved the application of multiple techniques, including the introduction of a novel switching algorithm to drive the Capacitive Digital-to-Analog Converter (CDAC) and the incorporation of redundancy in the SAR conversion steps. This redundancy increases the robustness of the SAR core against settling errors, enabling higher conversion speeds compared to binary implementations. The SAR core was fabricated in a 28-nm bulk CMOS process as an integral component of a 6× time-

interleaved converter. The presented sub-ADC is a 12-bit, 150-MS/s, 13-step redundant asynchronous SAR converter, achieving 63-dB Signal-to-Noise and Distortion Ratio (SNDR), which corresponds to 10.2 Effective Number Of Bits (ENOB), and 72- dB Spurious-Free Dynamic Range (SFDR), with an Equivalent Resolution Bandwidth (ERBW) larger than 100 MHz. To suppress the effects of time-interleave mismatches, the time-interleaved converter includes on-chip background calibrations. A novel skew calibration algorithm enables varying the number of active channels within the time-interleaved ADC, allowing adaptable signal bandwidth. This offers an interesting opportunity for optimizing the energy efficiency of multi-standard receivers. Despite the satisfying results, a degradation in the dynamic performance metrics was observed when transitioning from a single-core to a time-interleaved configuration. This degradation was primarily attributed to crosstalk between the channels through the shared reference distribution network, and to the absence of an on-chip input signal buffer. To address these impairments, a second prototype was designed, featuring a distributed reference buffer architecture that mitigates the channel interactions arising from the shared power supply and ground networks. Additionally, an input buffer with enhanced linearity was implemented to preserve the integrity of the input signal, mitigating the kickback of the input sampler of the ADC cores on the front-end network. The measurement results of this second prototype, a 2 GS/s 11-bit 8×-interleaved ADC, showcase an SNDR level consistent (within 1.4 dB) with the single-channel one across the entire 1 GHz input bandwidth, achieving 57.3 dB SNDR and 69.9 dB SFDR close to the Nyquist frequency.

Francesco TESOLIN – XXXV Cycle

PLL ARRAYS FOR PHASE NOISE REDUCTION AND BEAM STEERING

Supervisor: Prof. Salvatore Levantino

To meet the stringent requirements of next-generation communication standards, the demand for spectral purity in radio-frequency (RF) transceivers (TRX) has reached unprecedented levels. This challenge is exacerbated by the need for mass-volume production, which calls for the integration of complex baseband digita! signal processing (DSP) units into the same die as the TRX RF chain, typically implemented in scaled CMOS nodes. One of the most critical aspects of transceiver design is the local-oscillator (LO), typically realized as a phased-locked loop (PLL), which faces signif-icant challenges due to the voltage-supply scaling and the limited analog performance of devices in modem technologies. In particular, the voltage-controlled oscillator (VCO), or the digitally-controlled oscillator (DCO) in digital PLLs, exhibits a fundamental upper bound in phase-noise perfor-mance, that cannot be overcome even willing to increase power dissipa-tion. Multi-core oscillators have emerged as a promising solution to restare the traditional trade-off between power and phase-noise by leveraging the combination of different oscillator elements. However, to meet the specifications dictated by the increasingly demanding communication standards, a large number of oscillator cores should be used, making the design of a conventional PLL impractical, due to the lossy coupling network between the cores and the large quantity of connections required.
This research explores an alternative approach. Rather than employing multi-core oscillators within a single PLL loop, it leverages the combination of outputs from an array of PLLs to improve phase-noise performance. This enables the full optimization of each PLL core, while eliminating the challenges associated to the coupling networks and interconnections among oscillator cores. Moreover, adopting digital-PLLs (DPLLs) as core units allows to achieve, at a spectral purity

comparable to analog PLLs, a much smaller overall footprint with respect to the multi-core oscillator approach. Additionally, DPLLs offer the opportunity to implement new functionalities in each PLL element with minimal area and power effort. This research aims to unlock the potential of DPLL arrays for advanced communication systems.

The thesis is organized as follows:

- Chapter 1 introduces the challenges associated with PLL implemented in modem CMOS nodes and discusses the concept and limitations of multi-core-oscillator approach.
- Chapter 2 delves into phase-noise reduction through the adoption of DPLL arrays. Two distinct approaches are explored: the coupled PLL (CPLL), featuring a digital coupling path between adjacent elements in the array, and the output combinati on of PLL outputs through an on-chip power combiner. For the latter technique, a two-core prototype has been implemented, and the measurement results are presented.
- Chapter 3 discusses the inherent phase-shifting capability offractional-N digital PLLs to create an LO-phase-shifting system based on an ar-ray of DPLLs. When signals from multiple antennas are combined over-the-air, each equipped with an independent LO and uncorrelated noise sources, the combined signal experiences a reduction in phase noise. The chapter provides implementation details of the prototype and presents a complete set of measurement data to support the dis-cussion.

The main results of this research have been published in the following works divided in the following categories:

- Digital PLL arrays for phase noise reduction:

- Saleh Karman, Francesco Tesolin, Alessandro Dago, Mario Mercandelli, Carlo Samori, and Salvatore Levantino. "A 18.9-22.3GHz Dual-Core Digitai PLL with On-Chip Power Combination for Phase Noise and Power Scalability." In Proc. of 2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pages 67-70, 2021 [l].
- Saleh Karman, Francesco Tesolin, Salvatore Levantino, and Carlo Samori. "A Nove! Topology of Coupled Phase-Locked Loops." IEEE Transactions on Circuits and Sys-tems I: Regular Papers, 68(3):989-997, 2021 [2].
- Francesco Buccoleri, Simone M. Dartizio, Francesco Tesolin, Luca Avallone, Alessio Santiccioli, Agata Iesurum, Giovanni Steffan, Dmytro Cherniak, Luca Bertulessi, An-drea Bevilacqua, Carlo Samori, Andrea L. Lacaita, and Salvatore Levantino. "A 72-fs-

Total-Integrated-Jitter Two-Core Fractional- N Digitai PLL With Digitai Period Aver-aging Calibration on Frequency Quadrupler and True-in-Phase Combiner." IEEE Jour-nal ofSolid-State Circuits, pages 1-13, 2022 [3] .
- Francesco Buccoleri, Simone M. Dartizio, Francesco Tesolin, Luca Avallone, Alessio Santiccioli, Agata Lesurum, Giovanni Steffan, Andrea Bevilacqua, Luca Bertulessi, Dmytro Cherniak, Carlo Samori, Andrea L. Lacaita, and Salvatore Levantino. "A 9GHz 72fs-Total-lntegrated Jitter Fractional-N Digitai PLL with Calibrated Frequency Quadrupler." In Proc. of 2022 IEEE Custom Integrated Circuits Conference (CICC), pages 1-2, 2022 [4].

- Digitai PLL arrays with phase-shifting capabiiity:

- Francesco Tesolin, Simone M. Dartizio, Francesco Buccoleri, Alessio Santiccioli, Luca Bertulessi, Carlo Samori, Andrea L. Lacaita, and Salvatore Levantino. "A Novel LO Phase-Shifting

System Based on Digitai Bang-Bang PLLs With Background Phase-Offset Correction for Integrated Phased Arrays." IEEE Journal of So/id-State Circuits, 58(9):2466-2477, 2023 [5].

- Alessio Santiccioli, Mario Mercandelli, Simone M. Dartizio, Francesco Tesolin, Saleh Karman, Abanob Shehata, Luca Bertulessi, Francesco Buccoleri, Luca Avallone, An-gelo Parisi, Dmytro Cherniak, Andrea L. Lacaita, Michael P. Kennedy, Carlo Samori, and Salvatore Levantino. "32.8 A 98.4fs-Jitter 12.9-to-15. l GHz PLL-Based LO Phase-Shifting System with Digitai Background Phase-Offset Correction for Integrated Phased Arrays." In Digest of 2021 IEEE International Solid- State Circuits Conference (ISSCC), volume 64, pages 456-458, 2021 [6].

• High-spectrai-purity digitai PLLs:

- Simone M. Dartizio, Francesco Tesolin, Giacomo Castoro, Francesco Buccoleri, Luca Lanzoni, Michele Rossoni, Dmytro Cherniak, Luca Bertulessi, Carlo Samori, Andrea L. Lacaita, and Salvatore Levantino. "4.3 A 76.7fs-lntegrated-Jitter and -71.9dBc In-Band Fractional-Spur Bang-Bang Digitai PLL Based on an lnverse-Constant-Slope DTC and FCW Subtractive Dithering." In Digest of 2023 IEEE International Solid-State Circuits Conference (ISSCC), pages 3-5, 2023 [7].

- Giacomo Castoro, Simone M. Dartizio, Francesco Tesolin, Francesco Buccoleri, Michele Rossoni, Dmytro Cherniak, Luca Bertulessi, Carlo Samori, Andrea L. Lacaita, and Salvatore Levantino. "4.5 A 9.25GHz Digitai PLL with Fractional-Spur Cancellation Based on a Multi-DTC Topology." In Digest of 2023 IEEE International So/id-State Circuits Conference (ISSCC), pages 82-84, 2023 [7].

- Simone M. Dartizio, Francesco Buccoleri, Francesco Tesolin, Luca Avallone, Alessio Santiccioli, Agata Iesurum, Giovanni Steffan, Dmytro Cherniak, Luca Bertulessi, An-drea Bevilacqua, Carlo Samori, Andrea L. Lacaita, and Salvatore Levantino. "A Fractional−N Bang-Bang PLL Based on Type-11 Gear Shifting and Adaptive Frequency Switching Achieving 68.6 fs rrns-Total-Integrated-Jitter and 1.56 µs-Locking-Time." IEEE Jour-nal of So/id-State Circuits, 57(12):3538-3551, 2022 [8].

- Simone Mattia Dartizio, Francesco Buccoleri, Francesco Tesolin Luca Avallone, Alessio Santiccioli, Agata Iesurum, Giovanni Steffan, Dmytro Cherniak, Luca Bertulessi, An-drea Bevilacqua, Carlo Samori, Andrea Leonardo Lacaita, and Salvatore Levantino. A 68.6fsrms-total integrated-jitter and l.56µs-locking-time fractional-N bang-bang PLL based on type-11 gear shifting and adaptive frequency switching." In Digest of 2022 IEEE International So/id-State Circuits Conference (ISSCC), volume 65, pages 1-3, 2022 [9].

- Simone M. Dartizio, Francesco Tesolin, Mario Mercandelli, Alessio Santiccioli, Abanob Shehata, Saleh Karman, Luca Bertulessi, Francesco Buccoleri, Luca Avallone, Angelo Parisi, Andrea L. Lacaita, Michael P. Kennedy, Carlo Samori, and Salvatore Levantino. "A 12.9-to-15.1-GHz Digitai PLL Based on a Bang-Bang Phase Detector With Adap-tively Optimized Noise Shaping." IEEE Journal of Solid-State Circuits, 57(6):1723- 1735, 2022 [IO].

- Angelo Parisi, Francesco Tesolin, Mario Mercandelli, Luca Bertulessi, and Andrea L. Lacaita. "Self-Biasing Dynarnic Startup Circuit for Current-Biased Class-C Oscilla-tors." IEEE Microwave and Wìreless Components Letters, 31(9): 1075-1078, 2021 [11].

Francesco BUCCOLERI – XXXV Cycle

DIGITAL CONTROLLED OSCILLATORS: JITTER MINIMIZATION IN DIGITAL PHASE LOCKED LOOPS

Supervisor: Prof. Andrea Leonardo Lacaita

Over recent years, there has been a widespread adoption of wirelessconnected mobile devices in the consumer market. This can be attributed to the continuous advancements in data transmission speed and energy efficiency offered by contemporary transceivers. To keep pace with the growing demand for increased communication bandwidth, ongoing research endeavors have shifted their focus toward the implementation
of sophisticated modulation techniques at higher carrier frequencies. The use of high-order modulation techniques, on the other hand, creates more stringent phase-noise requirements for integrated frequency synthesizers. In addition, the relentless need for adaptive modulation hints to local oscillators (LOs) making use of noise and power scaling depending on the characteristics of the channel in order to maximize the efficiency of the system.
In this framework, the digital phase locked-loop (PLL) architecture is a promising candidate for the LO implementation, due to its lower power consumption and area occupation when compared to analog PLLs. The key building block in this system is the Digital Controlled Oscillator (DCO), being the bottleneck for jitter minimization. In recent decades, there has been a significant surge in interest in the field of DCO research, with a focus on comprehending the mechanics involved in the conversion of various noise sources. Currently, there is a comprehensive understanding of the factors that give rise to white noise contributions in the output phase. However, despite the considerable additional impact of flicker noise on overall jitter due to the relentless employment of deeply scaled CMOS technologies, there is still a lack of complete comprehension of the methods by which it is converted into phase noise. In addition, the practical implementation of a DCO is subject to physical constraints that limit its frequency resolution.
This limitation has a negative impact on the out-of-band performance of the
frequency synthesizer, mostly owing to the presence of significant quantization noise.
In this thesis, two viable solutions to overcome these limitations are presented. In addition, a theoretical analysis will be introduced to fulfill the gap in the understanding of the flicker noise conversion mechanism.
Firstly, an Integer-N bang-bang PLL (BBPLL) with a quadrupler-based oversampling technique aiming suppress the DCO quantization noise by introducing the lowest power overhead to the system. The use of the quadrupler is guaranteed by a digital period averaging calibration working in the background guaranteeing the proper functioning of the technique.
Secondly, a Fractional-N BBPLL based on a True-In-Phase Combiner (TIPC) enabling the possibility to reconfigure the system from a low-power mode to a low-jitter mode. This architecture guarantees not to affect the performances of the isolated DCOs thus ensuring the most efficient solution for re-configurable systems.
Lastly, a theoretical analysis of differential LC-oscillators is presented, aiming to quantify the relationship between oscillation frequency and the harmonic content of the oscillation waveform. This work expands upon Groszkowski's result, examining its generalization to differential oscillators and providing a sound estimation of flicker noise up-conversion mechanisms

PhD Committee

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