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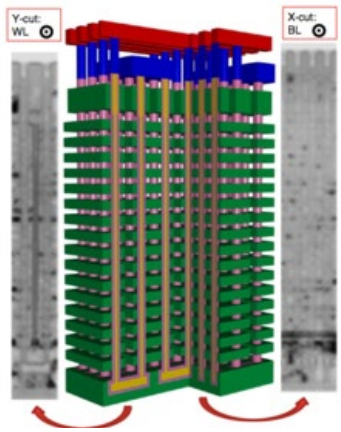
Seminar by Jian CHEN, Stanford University

History, Challenges and Opportunities on the IC Memory Lane: From 2D to 3D.

15 April 2024, at 11.15 in room 21.S.4

In our modern data-abundant digital world, memory technologies are becoming ever more important to fulfill ever lower cost, higher density, lower power, performance, functionality, and reliability. Two types of memory dominate the landscape, NAND for low-cost storage, and DRAM for fast main computing memory. This talk will share the history and current states of the technologies, how NAND has successfully transitioned from 2D to 3D with continued scaling path, and DRAM has reached scaling bottleneck, with possible but difficult transition to 3D on the horizon.



Currently an adjunct professor at Stanford, Jian Chen was senior VicePresident of Technology development for SanDisk's 3D NAND technology from 2013 to 2020. Prior to that, he was VP of Memory System Engineering leading the design of emerging memory system architectures and of SD/uSD and SSD products. He was the first device/process engineer to work on the SanDisk-Toshiba joint NAND venture in 1999,. With 150+ granted US patents, he invented some of the fundamental patents in NAND device/process and systems that are been used for over 10 generations of NAND products.